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WE CLAIM:

1. A packet-switched system for communicating data, comprising:

a plurality of packet transmitters, each packet transmitter including,

a transmitter-first-in-first-out (transmitter-FIFO) memory, coupled to a data input, for storing data;

an encoder, coupled to said transmitter-FIFO memory, for encoding the data from said transmitter-FIFO memory as encoded data;

a demultiplexer, coupled to said encoder and having a plurality of outputs, for demultiplexing the encoded data into a plurality of sub-data-sequence signals, with a respective sub-data-sequence signal at a respective output of said demultiplexer;

chip-sequence means for outputting a plurality of chip-sequence signals, with each chip-sequence signal orthogonal to the other chip-sequence signals in said plurality of chip-sequence signals;

a plurality of product devices, coupled to the plurality of outputs of said demultiplexer, respectively, and to said chip-sequence means, for multiplying each of the sub-data-sequence signals by a respective chip-sequence signal, thereby generating a plurality of spread-spectrum channels;

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LAW OFFICES
DAVID NEWMAN
& ASSOCIATES, P.C.
CENTENNIAL SQUARE
P.O. BOX 2728
LA PLATA, MD 20646
(301) 934-6100

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a combiner, coupled to the plurality of product devices, for algebraically combining the plurality of spread-spectrum channels as a multichannel-spread-spectrum signal;

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a header device, coupled to said combiner, for concatenating a header for chip-sequence synchronization, to the multichannel-spread-spectrum signal, thereby generating a packet-spread-spectrum signal; and

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a transmitter subsystem, coupled to said header device, for transmitting on a carrier frequency the packet-spread-spectrum signal using radio waves over a communications channel; and

a plurality of packet receivers, each packet receiver including,

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a translating device, coupled to the communications channel, for translating the packet-spread-spectrum signal from the carrier frequency to a processing frequency;

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a header-matched filter, coupled to said translating device and having an impulse response matched to the header, for detecting, at the processing frequency, the header in the packet-spread-spectrum signal, and for outputting, responsive to detecting the header, a header-detection signal;

a processor, coupled to said header-matched filter, responsive to the header-detection signal, for generating control and timing signals;

55 a plurality of data-matched filters, coupled to
said translating device, with each data-matched filter
having an impulse response matched to a chip-sequence
signal of the plurality of chip-sequence signals,
respectively, for despreding the multichannel-spread-
spectrum signal embedded in the packet-spread-spectrum
signal as a plurality of received spread-spectrum channels,
respectively;

60 a multiplexer, coupled to said plurality of data-
matched filters, for multiplexing the plurality of received
spread-spectrum channels as received-encoded data;

a decoder, coupled to said multiplexer, for
decoding the received-encoded data as received data; and

65 a receiver-FIFO memory, coupled to said decoder,
for storing the received data, and for outputting the
received data to a data output.

2. The packet-switched system as set forth in claim 1,
with said chip-sequence means including a chip-sequence
generator for generating the plurality of chip-sequence signals.

3. The packet-switched system as set forth in claim 1,
with said chip-sequence means including a memory for storing the
plurality of chip-sequence signals.

4. A packet-switched system for communicating data, comprising:

a plurality of packet transmitters, each packet transmitter including,

transmitter-memory means, coupled to a data input, for storing data;

encoder means, coupled to said transmitter-memory means, for encoding the data from said transmitter-memory means as encoded data, with the data from each packet transmitter encoded differently from the data from other packet transmitters in said plurality of packet transmitters;

demultiplexer means, coupled to said encoder means and having a plurality of outputs, for demultiplexing the encoded data into a plurality of sub-data-sequence signals, with a respective sub-data-sequence signal at a respective output of said demultiplexer means;

spread-spectrum means, coupled to the plurality of outputs of said demultiplexer means, for spread-spectrum processing each of the sub-data-sequence signals by a respective chip-sequence signal, thereby generating a plurality of spread-spectrum channels, with the respective chip-sequence signal different from a each chip-sequence signal in a plurality of chip-sequence signals for spread-spectrum processing the plurality of sub-data sequence signals, respectively, and with the plurality of chip-sequence signals commonly used by the plurality of packet

transmitters;

combiner means, coupled to the spread-spectrum means, for algebraically combining the plurality of spread-spectrum channels as a multichannel-spread-spectrum signal;

header means, coupled to said combiner means, for adding a header for chip-sequence synchronization, to the multichannel-spread-spectrum signal, thereby generating a packet-spread-spectrum signal; and

transmitter means, coupled to said header means, for transmitting at a carrier frequency the packet-spread-spectrum signal using radio waves over a communications channel; and

a plurality of packet receivers, each packet receiver including,

header-detection means, coupled to said communications channel, for detecting the header in the packet-spread-spectrum signal, and for outputting, responsive to detecting the header, a header-detection signal;

receiver-spread-spectrum means, coupled to said header-detection means, for despreading the multichannel-spread-spectrum signal embedded in the packet-spread-spectrum signal as a plurality of received spread-spectrum channels, respectively;

multiplexing means, coupled to said receiver-spread-spectrum means, for multiplexing the plurality of received spread-spectrum channels as received-encoded data;

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decoding means, coupled to said multiplexing means, for decoding the received-encoded data as received data; and

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receiver-memory means, coupled to said decoding means, for storing the received data, and for outputting the received data to a data output.

5. The packet-switched system as set forth in claim 4, further including translating means, coupled between the communications channel and the header-detection means, for translating the packet-spread-spectrum signal from the carrier frequency to a processing frequency.

6. The packet-switched system as set forth in claim 4, further including processor means, coupled to said header-detection means, responsive to the header-detection signal, for generating control and timing signals.

7. The packet-switched system as set forth in claim 4, 5 or 6 with said spread-spectrum means including:

generating means for generating the plurality of chip-sequence signals; and

a plurality of EXCLUSIVE-OR gates coupled between said demultiplexing means, said combiner means and said generating means, for multiplying the plurality of sub-data-sequence signals by the plurality of chip-sequence signals, respectively, thereby generating the plurality of spread-spectrum channels.

8. The packet-switched system as set forth in claim 4, 5 or 6 with said spread-spectrum means including a memory for storing the plurality of chip-sequence signals.

9. The packet-switched system as set forth in claim 4, 5 or 6 with said encoding means including any of an encryptor and a privacy device.

10. The packet-switched system as set forth in claim 4, 5 or 6 with said spread-spectrum-processing means including a plurality of product devices for multiplying each of the sub-data-sequence signals by a respective chip-sequence signal of the plurality of chip sequence signals.

11. The packet-switched system as set forth in claim 4, 5 or 6 with said spread-spectrum means including a plurality of matched filters, with each matched filter having an impulse response matched to a chip-sequence signal of the plurality of chip-sequence signals, respectively.

12. The packet-switched system as set forth in claim 4, 5 or 6 with said spread-spectrum means including a plurality of surface-acoustic-wave devices, with each surface-acoustic-wave device having an impulse response matched to a chip-sequence signal of the plurality of chip-sequence signals, respectively.

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13. The packet-switched system as set forth in claim 4, 5 or 6 with said receiver-spread-spectrum means including a plurality of data-matched filters, with each data-matched filter having an impulse response matched to a chip-sequence signal of the plurality of chip-sequence signals, respectively.

14. The packet-switched system as set forth in claim 4 with said receiver-spread-spectrum means including a plurality of surface-acoustic-wave devices, with each surface-acoustic-wave device having an impulse response matched to a chip-sequence signal of the plurality of chip-sequence signals, respectively.

15. The packet-switched system as set forth in claim 4 with said header-detection means including a header-matched filter having an impulse response matched to the header.

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